IN THE CLAIMS

Claims *1-15* are pending in this application. Please cancel claims *1-4, 8 and 10-13* without prejudice or disclaimer, amend the remaining claims, and add new claims *16 and 17* as follows:

1-4. (Canceled).

5. (Currently Amended) A semiconductor integrated circuit comprising:

a first bus;

a second bus;

a data transfer ~~device~~ unit to transfer data between the first bus and the second buses;

a central processing unit connected to the first bus; ~~and~~

~~program storage memory which stores a control program for the central processing unit and is~~ a first module connected to the first bus[,];

a second module connected to the second bus; and

a bus control unit controlling bus arbitration for the first bus and the second bus,

~~wherein~~ the data transfer unit ~~device can independently request a bus access right and output an address to the first and second buses, the device~~ requesting[~~s~~] a bus access right of one of the buses for reading to the bus control unit, accessing the one bus for reading data, and releasing the bus access right of the one bus, and

requesting[~~s~~] a bus access right of the other bus for writing ~~at a different timing~~ to the bus control unit after releasing the bus access right of the one bus and accessing the other bus for writing the data in response to one data transfer start request, ~~and~~

~~wherein~~ the central processing unit ~~is~~ being capable of bus access to the first module using the first bus in parallel with bus access to the second module using the second bus by ~~means of~~ the data transfer ~~device~~ unit in response to one data transfer start request.

6. (Currently Amended) A semiconductor integrated circuit comprising:

a first bus;

a second bus;

a data transfer ~~device~~ unit to transfer data between the first bus and the second buses~~;~~

a central processing unit connected to the first bus; and

a bus control ~~means~~ unit controlling bus arbitration for the first bus and the second buses~~,~~

~~wherein~~ the data transfer ~~device~~ unit ~~can~~ being capable of independently requesting a bus access right and output an address to the first bus and the second buses according to a data transfer start request, requesting[~~s~~] a bus access right of one of the buses for reading to the bus control unit, accessing the one bus according to the bus access right of one bus and releasing the bus access right of one bus, and requesting[~~s~~] a bus access right of the other bus for writing ~~at a different timing in response to one data transfer start request~~ after accessing the one bus for reading, ~~and wherein~~ the bus control ~~means~~ unit ~~is~~ being capable of arbitration of bus access right requests and bus control for the first bus and the second buses independently in response to the one data transfer start request.

7. (Currently Amended) A semiconductor integrated circuit comprising:

a first bus;

a second bus;

a third bus;

a central processing unit connected to the first bus;

program storage memory which stores a control program for the central processing unit and is connected to the first bus; ~~and~~

a data transfer device capable of data transfer between the second bus and the third buses~~;~~ and

a bus control unit for controlling the first bus, the second bus, and the third bus, ~~wherein~~ the data transfer device ~~can~~ being capable of independently request a bus access right and output an address to the second bus and the third buses~~,~~ ~~the device~~ requesting[~~s~~] a bus access right of one of the buses for reading, accessing to the one bus according to the bus access right, and releasing the bus access right of one bus,

and requests a bus access right of the other bus for writing ~~at a different timing~~ in response to one data transfer start request, ~~and~~

~~wherein the central processing unit is capable of bus access using the first bus in parallel with bus access using the second or third bus by means of the data transfer device~~

the bus control unit being capable of arbitration of bus access right requests and bus control for the first bus, the second bus, and the third bus independently.

8. (Canceled).

9. (Currently Amended) The semiconductor integrated circuit according to claim ~~8~~7,

wherein the central processing unit can access the second bus or the third bus from the first bus via the bus control ~~means~~ unit.

10-13. (Canceled).

14. (Currently Amended) The microcomputer according to claim ~~10~~ 7,

wherein the data transfer device has a plurality of data transfer channels and a control register to specify data transfer channel operations, and

wherein the control register has a transfer request generation source specification area for defining correspondence between a data transfer channel to receive a transfer request and a transfer request generation source; a source bus specification area for defining correspondence between a data transfer channel and a transfer source bus; and a destination bus specification area for defining correspondence between a data transfer channel and a transfer destination bus.

15. (Original) The microcomputer according to claim 14,

wherein a central processing unit can access the control register.

16. (New) The semiconductor integrated circuit according to claim 5,

wherein the bus control unit is capable of arbitration of bus access right requests and bus control for the first bus and the second bus independently in response to the one data transfer start request.

17. (New) The semiconductor integrated circuit according to claim 6,

wherein the central processing unit is capable of bus access to the first module using the first bus in parallel with bus access to the second module using the second bus by the data transfer unit in response to one data transfer request.